IN THE CLAIMS:

Please enter the following amended claim:

1 (original): A flexible chip stacked chip assembly comprising:

a plurality of chips (100, 110, 120) folded over one another and flexibly connected to one another by discrete insulated interconnects (40); and

one chip (130) mounted on a chip carrier (500) flexibly connected to said plurality of folded chips (100, 110, 120) providing electrical connection between said plurality of stacked chips to pads (510) on said chip carrier (500).

2 (original): The flexible chip stacked chip assembly recited in claim 1, wherein said discrete insulated interconnects are made of a conductive material selected from the group consisting of aluminum and copper.

3 (currently amended): The flexible chip stacked chip assembly recited in claim 1 wherein [[the]] a length of said interconnects is determined by the order in which the chips are folded.

4 (original): The flexible chip stacked chip assembly recited in claim 1 further comprising a thermal conduit folded into said plurality of folded stacked chips to provide means for extracting waste heat generated by said plurality of folded stacked chips.

5 (original): The flexible chip stacked chip assembly recited in claim 4 wherein at least one chip makes physical connection to said thermal conduit.

6 (currently amended): The flexible chip stacked chip assembly recited in claim 1 wherein [[the]] a bottom surface of the first chip of said ~~plurality~~ assembly faces the bottom surface of the second chip of said assembly, while the bottom of the third chip faces the top of the second chip of [[the]] said assembly.

7 (original): The flexible chip stacked chip assembly recited in claim 1 wherein said plurality of chips (100, 110, 120) is arranged with the chips positioned substantially parallel with one another.

8 (original): The flexible chip stacked chip assembly recited in claim 1 wherein said chip carrier (500) is selected from the group consisting of a silicon substrate, a system-on-package, a transposer, and a printed circuit board

9 (original): The flexible chip stacked chip assembly recited in claim 1 wherein said plurality of stacked chips is arranged in a non-parallel chip arrangement.

10 (currently amended): A flexible chip stacked chip assembly comprising:

a plurality of chips (100, 110, 120) flexibly folded over one another and connected to one another by flexible discrete insulated interconnects (40), wherein the bottom most ~~bottommost~~ chip (110) is provided with a grid array of solder balls (550) making electrical contact between said plurality of stacked chips to pads on a chip carrier (600).

11 (original): The flexible chip stacked chip assembly recited in claim 10 further comprising a thermal conduit snaking between said plurality of stacked chips.

12 (currently amended): The flexible chip stacked chip assembly ~~same as~~ recited in claim 11 wherein at least one chip of said plurality of stacked chips (100, 110, 120) makes physical connection to said thermal conduit.

13 (original): An array of multi-chip assemblies comprising:

a plurality of flexible stacked chip assemblies, each of said assemblies respectively comprising a plurality of chips (100, 110, 120) folded over one another and connected to one another by flexible discrete insulated interconnects, wherein at least one of said flexible chip assemblies is attached to a chip carrier (500).

14 (original): The array of multi-chip assemblies recited in claim 13 wherein said chip carrier (500) is selected from the group consisting of a silicon substrate, a system-on-package (SOP), a multi-chip module and a transposer.

15 (original): The array of multi-chip assemblies recited in claim 13 further comprising a thermal conduit folded within said plurality of folded stacked chips to provide means for extracting waste heat generated by said plurality of folded stacked chips.

16 (original): A method of forming a flexible chip stacked chip assembly comprising the steps of:

folding a plurality of chips (100, 110, 120) over one another, connecting one chip of said plurality of chips (100, 110, 120) to another by flexible discrete insulated interconnects (40) ; and

mounting at least one chip on a chip carrier (500) electrically coupled to said plurality of folded chips to provide electrical connection between said plurality of stacked chips to pads (510) on said chip carrier (500).

17 (original): A method of providing a flexible chip stacked chip assembly comprising the steps of:

folding a plurality of chips (100, 110, 120) over one another, connecting one chip of said plurality of chips (100, 110, 120) to another by flexible discrete insulated interconnects, wherein the bottommost chip (110) of said plurality of chips (100, 110, 120) is provided with a grid array of solder balls making electrical contact between said plurality of stacked chips to pads (510) on a chip carrier (500).

18 (original): A method of constructing an array of multi-chip assemblies comprising the steps of:

providing a plurality of flexible stacked chip assemblies, each of said assemblies respectively comprising a plurality of chips (100, 110, 120) folded over one another and connected to one another by flexible discrete insulated, wherein at least one of said one of said flexible chip assemblies is attached to a chip carrier (500).